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EFFECTS OF ANNEALING TEMPERATURE ON THE CRYSTALLOGRAPHIC, MORPHOLOGICAL AND ELECTRICAL CHARACTERISTICS OF E-BEAM DEPOSITED Al/Eu_2O_3/N-Si (MOS) CAPACITORS

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Abstract. *Rare earth oxides (REOs) play an important role in the semiconductor technology. Europium oxide (Eu_2O_3) is one of REOs and it has been used in many applications such as optoelectronics, telecommunications, microelectronics and optical devices. However, in this study, Eu_2O_3 MOS capacitors have been fabricated by using the Electron Beam Evaporation (E-Beam) technique and the effects of different annealing temperatures on them have been investigated. Before and after annealing, the crystallographic and morphological properties of the Eu_2O_3 films have been analyzed by X-ray Diffraction and Atomic Force Microscopy. The electrical properties of the devices have been investigated using measuring C-V, G/ω-V characteristics. This preliminary study shows that Europium oxide can be suitable for application as a thin film.*

Keywords: *Europium Oxide, MOS structure, Capacitance-Voltage, Conductance-Voltage*

1. Introduction

Metal-oxide-semiconductor (MOS) capacitors have a very important role in microelectronic applications [1]. The SiO_2 layer is conventionally used in MOS-based devices [1], [2]. However, for the last few decades, rare earth oxides (REOs), such as Er_2O_3, Yb_2O_3, Gd_2O_3, Dy_2O_3, and Y_2O_3 [3]–[8], draw attention in the field of microelectronics. The REOs have lots of properties that can be used as a gate dielectric when their performance compares with SiO_2. Among those properties are wide bandgap (E_g=4-6 eV), high dielectric constant (ε=7-20), high recrystallization temperature, thermodynamic stability, high-quality interface with Si with low interfacial state density, and lower leakage conduction than SiO_2 at an equivalent oxide thickness. Europium oxide (Eu_2O_3) is one of REOs and it has features such as high dielectric constant (ε=14) [9], large energy band gap (E_g=4.4 eV) [10], [11], high chemical durability and thermal stability [12]. In the account of these properties, Eu_2O_3 has some advantages compared to a silicon dioxide (SiO_2) as a gate dielectric in many applications such as optoelectronics, telecommunications, microelectronics, and optical devices [9].

In this study, Eu_2O_3 MOS capacitors have been fabricated by using the Electron Beam Evaporation (E-Beam) technique and the effects of different annealing temperatures on them have been investigated. The C–V and G/ω–V measurements of the generated Eu_2O_3 MOS capacitor were measured at 1 MHz.

2. Experimental procedure

Europium oxide thin film was deposited onto a 500 μm thick n-type silicon (n-Si) wafer with a resistivity of 2-4 Ω cm by the E-Beam deposition technique. Before the deposition of the oxides, the wafer was cleaned by following the standard radio corporation of America's (RCA) cleaning procedures. The 99.99% pure Eu_2O_3 granules were used as target material during the film deposition. The base chamber pressure and the substrate temperature were adjusted to below 7.4×10−4 Pa and 150°C, respectively, before the Eu_2O_3 deposition. The thickness of the europium oxide is approximately determined to be 40 nm with the Spectroscopic Ellipsometer (AngstromSun Technology-Sr100). Then, this wafer was cut into five pieces. One of them was kept as deposited and the others were annealed at 300◦C, 500◦C, 700◦C, and 900◦C in a N_2 environment for 40 min, respectively. The chemical characteristics of the Eu_2O_3/n-Si structure were determined by a Perkin Elmer Spectrum Two FTIR-ATR (Fourier Transform İnfraRed – Attenuated Total Reflectance) spectrophotometer. The crystallographic of Eu_2O_3 thin film was analyzed by a Rigaku Multiflex diffractometer employing CuKα radiation while the morphological change of Eu_2O_3 thin film depending on annealing temperatures was studied by Atomic Force Microscopy.

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In order to make the front and back contacts of these devices (Fig.1), the aluminum (Al 99.999%) sputter target was used. The process and sputtering pressures were adjusted below 7.0 × 10−4, and 1 Pa, respectively. The capacitance–voltage and conductance–voltage for the fabricated Al/ Eu_2O_3/n-Si MOS capacitors were obtained at 1 MHz at room temperature using Impedance Analyzer (MODEL HIOKI 3532-50 LCR meter).

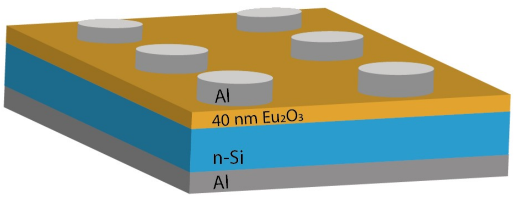

Figure 1. Schematic structure of the Al/Eu_2O_3/n-Si/Al MOS capacitor.

3. Results and Discussion

3.1. FTIR, XRD, and AFM results

The FTIR spectrum of Eu_2O_3 on Si after annealing at as-deposited and different temperatures can be seen as Figure 2. The peaks (at 2335 cm^{-1}, 2100 cm^{-1}, 1992 cm^{-1}, 1240 cm^{-1}, and 1110 cm^{-1}) of Eu_2O_3 thin films are getting smaller with increasing of annealing temperature, while it is observed that some small peaks emerge between 840 cm^{-1} and 700 cm^{-1}. These peaks are related to the Eu-O bending modes[13], [14].

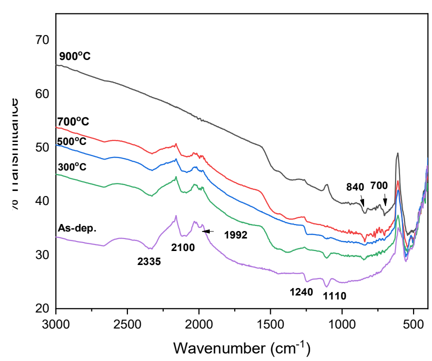

Figure 2. FTIR spectra of Eu_2O_3 /Si thin films at different annealing temperatures.

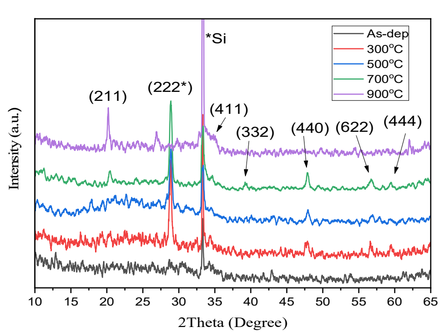

Figure 3. The XRD pattern of the Eu_2O_3/Si structure as-deposited and annealed at 300 °C, 500 °C, 700 °C, 900 °C.

The diffraction patterns of the annealed thin films (Fig. 3) can be indexed to the cubic phase, which is consistent with the values in the standard card (JSPDS no. 34-0392, quality «*», a value of 10.86 nm) [15], [16]. The grain size (D) of the film was calculated using Debye-Scherrer formula [17].

$$D = \frac{0.9 * \lambda}{\beta \cos \theta} \quad (1)$$

The values of grain size and crystallinity of the films increase with the increasing annealing temperatures, except for 900°C annealed sample[18], [19] (Table 1).

Table 1. Grain size (nm), Crystallinity (%), and RMS Roughness (nm) of deposited Eu_2O_3/Si depend on annealing.

Annealing Temp.(°C)	Grain size (nm)	Crystallinity (%)	RMS Roughness (nm)
As-deposited	-	-	0.135
300	23.69	15.70	0.156
500	24.28	15.81	0.200
700	26.45	29.39	0.238
900	12.15	18.01	0.664

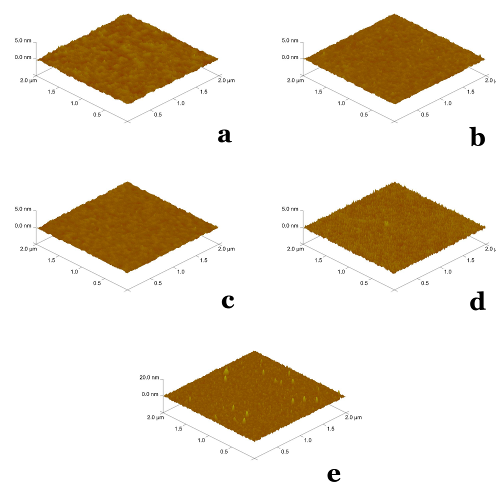

Figure 4. The AFM pictures of the Eu_2O_3/Si structure a) as- deposited and annealed at b) 300 °C, c) 500 °C, d) 700 °C, e) 900 °C.

The effects of annealing temperature on the surface morphology of the Eu_2O_3 thin films were investigated by AFM measurements (Fig. 5). Although there is no obvious effect of the annealing in the obtained measurements, the slight rises in the root-mean-square (RMS) roughness that have been observed by calculating in the AFM analysis program (Table 1) [12], [20].

3.2. Electrical characteristics results

The electrical properties of Eu_2O_3 MOS capacitor were investigated by capacitance-voltage and conductance–voltage measurements at the 1MHz (Fig. 5, a and b). The graphs of the C-V and G/w-V analyses show an increasing trend with the increasing annealing temperature up to the annealed sample at 900 °C. This phenomenon can appear because of the recovery of stoichiometry that results in the reduction of structural defects [21], [22]. On the other hand, the condition of the sample annealed at 900 °C can be owing to the phase transition depending on the annealing temperature [19], [23].

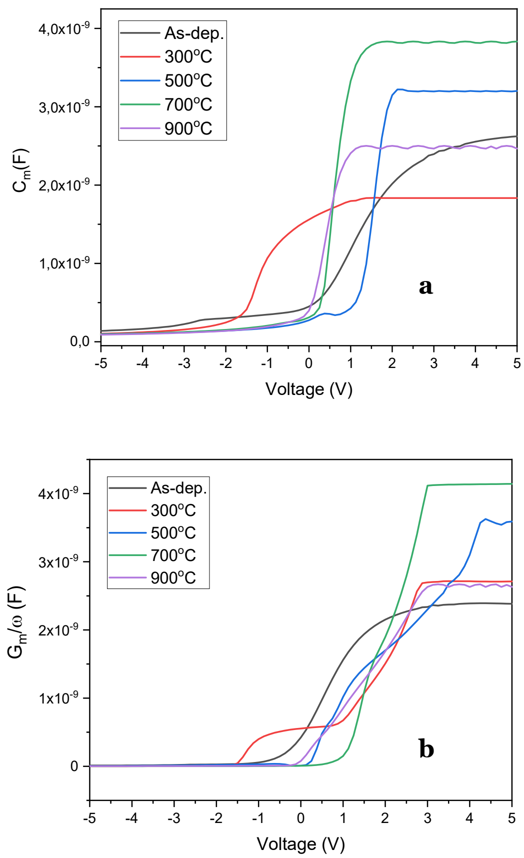

Figure 5. The electrical (a) C-V and (b) G/ω-V characteristics of Al/Eu_2O_3/Si/Al MOS capacitors at 1MHz.

4. Conclusion

In this study, Eu_2O_3 MOS capacitors have been fabricated by using the Electron Beam Evaporation (E-Beam) technique. The effects of different annealing temperatures on them have also been investigated. The crystallinity of Eu_2O_3 thin films is sensitive to the annealing, while the grain size of films slightly increases with annealing temperature increase. The results of ATR-FTIR measurements show some changes in the structure of Eu_2O_3 thin film because of the annealing. The process of annealing was caused by a small increase in the RMS values of Eu_2O_3 thin films found using AFM analysis. The annealing has been shown to be effective on the electrical properties of the Eu_2O_3 MOS capacitor. The measurement capacitance and the measurement conductance of Eu2O3 MOS capacitors increase with the annealing temperature increase.

The results show that Eu_2O_3 rare earth materials can be good candidates for microelectronic applications, but more detailed research is required on this rare earth oxide.

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