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INVESTIGATION OF ANNEALING TEMPERATURE ON STRUCTURAL, MORPHOLOGIES AND ELECTRICAL PROPERTIES Al/Y_2O_3/SiNWs/N-Si MOS CAPACITOR

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Abstract. *In this paper, we report the influence of post deposition annealing temperature on structural, morphological, and electrical properties of silicon nanowires (SiNWs) with Y_2O_3. SiNWs were fabricated by metal assisted chemical etching (MACE) method at room temperature. After the fabrication process, the high-k of Y_2O_3 was deposited onto SiNW/n-Si(100) by e-beam evaporation technique. Three samples of Y_2O_3 with SiNWs were annealed at 200°C, 400°C and 600°C in N_2 ambient for 40 min, while one sample was kept as deposited, respectively. The crystalline and morphological properties of Y_2O_3/SiNWs/n-Si(100) were analyzed by XRD and SEM techniques. On the other hand, the electrical properties of the capacitors based on SiNWs were investigated through C-V measurements at 1MHz. We found that the capacitance value in the accumulation region, dielectric constant(k) and interface states density (N_{it}) decreased with an increase in the annealing temperature. This could be attributed to the formation of interfacial layer and dangling bonds during high annealing temperature.*

Keywords: *post deposition annealing temperature; SiNWs; MACE; C-V; XRD; SEM*

1. INTRODUCTION

One–dimensional (1D) semiconductor nanomaterials such as silicon nanowires (SiNWs) have received considerable attention in recent years, as these materials have unique electrical, chemical, magnetic, and optical properties, which are different from bulk material properties[1]–[4]. Research in this area is motivated by the possibility of designing semiconductor nanomaterials with applications leading to technological advances in radiation sensors, photovoltaic cell, thermoelectric, lithium-ion batteries, and areas of medical research [2], [3].

Since manageable production of silicon nanowire is necessity for their device application,various ways of controlled fabrication of silicon nanowires have been implemented such as vapour liquid solid (VLS) growth method, molecular beam epitaxy growth method, laser ablation, and metal assisted chemical etching (MACE) method [3], [4]. Among them, MACE is one of the simplest methods for the fabrication of SiNWs due to its low cost, large surface area, and good repeatability. Moreover, SiNWs fabricated by this method have good crystalline quality [3]–[6].

Post deposition annealing (PDA) temperature is well known treatment and has been used in various technological industries for the improvement of stoichiometry oxides and their interface states of the fabricated devices [6], [7]. This can have a huge impact on the electrical characteristics of the devices at large. However, there is no report in the literature about the influence of annealing temperature on the SiNWs with Y_2O_3 [7], [8].Despite several efforts have been focused on annealing effects of SiNWs based solar cells with Al_2O_3 and SiNWs nanocomposite with P_3HT [6]. Therefore, exploiting the possible mechanisms of annealing effects on structural and morphology properties of SiNWs with Y_2O_3 will help us understand various phenomena in the structure and it can be beneficial for various fields such as solar energy, sensors, and electronic devices.

Therefore, in this current work, we report the effect of PDA on the structural, morphological, and electrical properties of SiNWs with Y_2O_3. The obtained results have been discussed in detail and compared with those results reported by previous researchers.

2. EXPERIMENTAL DETAILS

In this work, we report the fabrication of SiNWs based MOS capacitors and the experimental details can be divided as follows. First, n-type Si (100) wafers which had a resistivity of 2-4Ωcm were cleaned using RCA cleaning process. Second, the samples were immersed in a mixed solution of $AgNO_3$/HF/H_2O (0.0064g/29ml/121ml) for 90 seconds for the formation of AgNPs. Third, the samples were dipped in an etching solution which contained of HF/H_2O_2/H_2O (12ml/3ml/120ml) for 18 minutes. Fourth, the samples were submerged into the mixture of HNO_3/H_2O (20ml/20ml). This was done for removing of AgNPs on the surface of the samples. Before the deposition of Y_2O_3 thin films, the samples were immersed into a mixed solution of HF/H_2O for 20 sec to get rid of the oxide that

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might grow during the fabrication of the SiNWs. Moreover, each step the samples were rinsed with water for several times and then dried under N_2.

The samples were then loaded into a magnetron sputtering technique for the deposition of Y_2O_3 thin films. Then, Y_2O_3 thin films were deposited onto SiNWs/n-Si(100)under the experimental conditions of substrate temperature 250 °C, chamber pressure ~ 5.5×10^{-4} Pascal (Pa), the pre-sputter was performed at 1hr 30min to remove the impurities on the target, and sputtering time was 30min and sputtering power was set at 250W. After the deposition process, the thickness of Y_2O_3 was measured by Sun Spectroscopy Ellipsometry technique and found to be 150nm. The samples were again loaded into a RF magnetron sputtering to produce MOS capacitors. The front gate was formed using Aluminium as a sputtering target and the back contact was also formed with similar condition and for more details readers are referred to [9]. Subsequently, the MOS capacitors were divided into four parts, while one was left out as- deposited and three were annealed at different temperature of 200°C, 400°C and 600°C for 40 min in N_2 ambient. The crystalline structure and surface morphology of the SiNWs were investigated by XRD and SEM techniques. The capacitance-voltage (C-V) measurements were performed at 1MHz in the voltage range of -10V to +10 with a help of Keithly -4200 Semiconductor Characterization System (SCS).

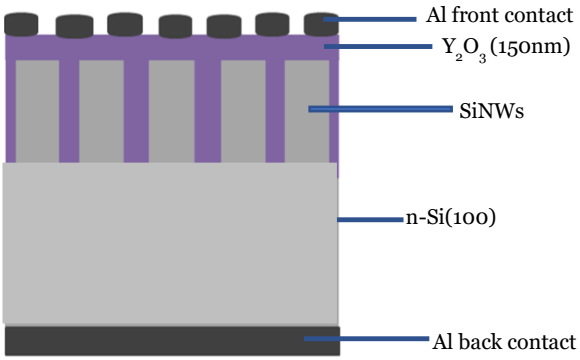


Figure 1. Structure of Al/Y_2O_3/SiNWs/n-Si (100) MOS capacitor.

3. Results and Discussions

3.1. Crystalline structure, elemental composition, and surface morphologies analysis

The XRD patterns of as deposited and annealed samples at 200°C, 400°C and 600°C of Y_2O_3/SiNWs are given in Figure 2. As can be seen in the XRD pattern of as-deposited sample only one peak is present at 2θ=30.4° with corresponding orientation of (222). However, the sample which was annealed at 200°C, had only two peaks at 2θ=33.69° and 48.8° with indexed of (400) and (440). As the annealing temperature increased up to 400°C, the sample turned into amorphous, in other words no peak was present. Furthermore, as the annealing temperature increased up to 600°C, the peaks were found at 2θ= 21.83° and 57.9° with the preferred orientation of (211) and (622). All these peaks in the XRD patterns belong to the Y_2O_3 thin films. On the other hand, we could not find any peak belonging to Ag and this could be attributed to the presence of HNO_3 in the solution during the last step for fabrication of SiNWs and similar results were observed [10]. Also, EDS analysis support these results as shown in Figure 3.

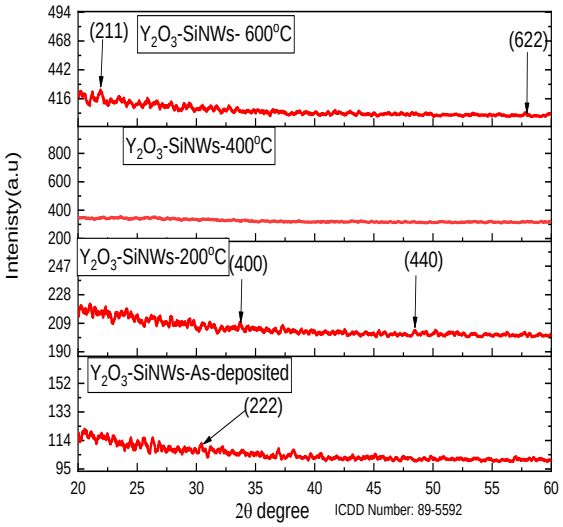
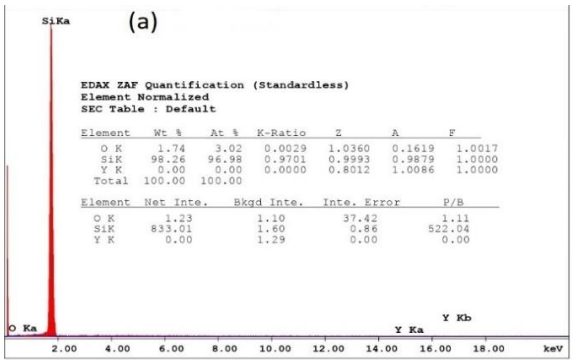


Figure 2. XRD patterns of as deposited and annealed samples at 200°C, 400°C and 600°C of Y_2O_3/SiNWs.

Energy dispersive x-ray spectroscopy (EDS) method was employed to study the elemental compositions which were present in the Y_2O_3/SiNWs/n-Si(100) for as-deposited and annealed samples at 200°C, 400°C and 600°C. As shown in all the figures, EDS confirms the elements are O, Si and Y. In all the EDS spectra. It can be observed that oxygen and silicon have emission X-ray signals at K_a at 0.64eV and 1.75eV while yttrium has K_a at 14.23eV and K_b at 15.1eV. On the other hand, the net intensity for oxygen element decreased with an increase in the annealing temperature as seen from the figures.



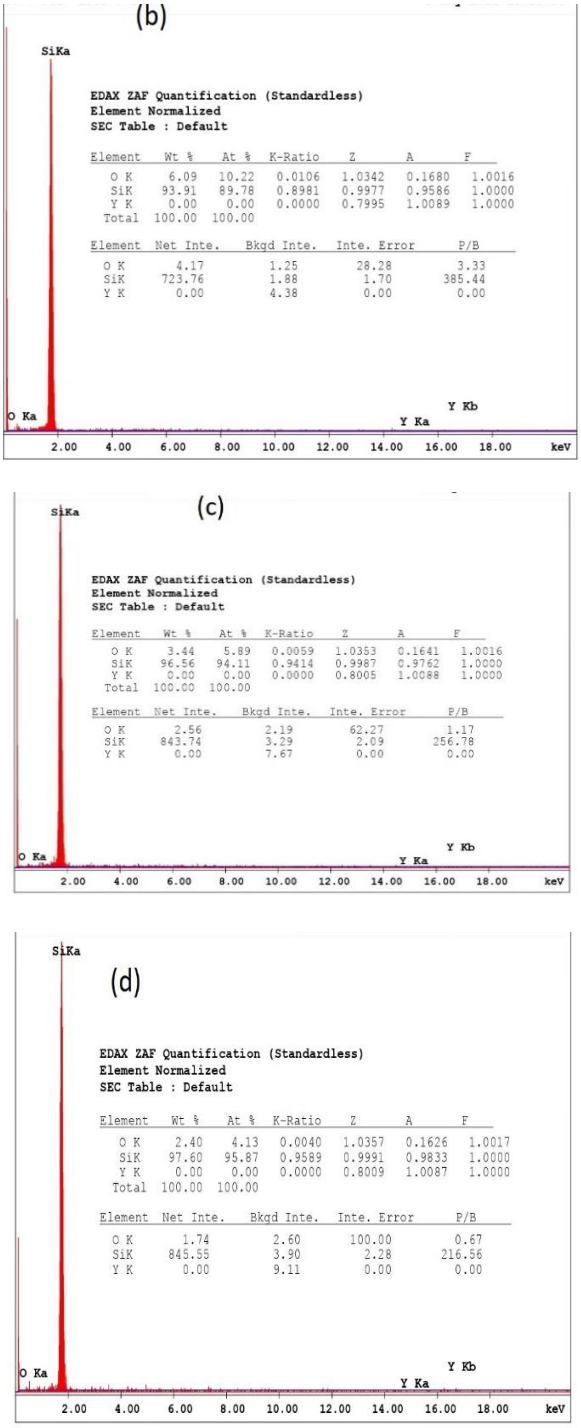


Figure 3. EDX spectra of Y_2O_3 thin films after deposition onto SiNWs/n-Si(100) for (a) as-deposited and annealed samples at (b) 200°C, (c) 400°C and (d) 600°C in N_2 for 40min.

Figure 4 shows cross-sectional and top views SEM images of SiNWs covered with Y_2O_3 thin films for as deposited and annealed samples at 200°C, 400°C, and 600°C. It is discoverd that the surface morphologies for sample annealed at 400°C reduces significantly compared to other samples. This could be related to the formation of dangling bonds during high annealing temperature [4], [6].

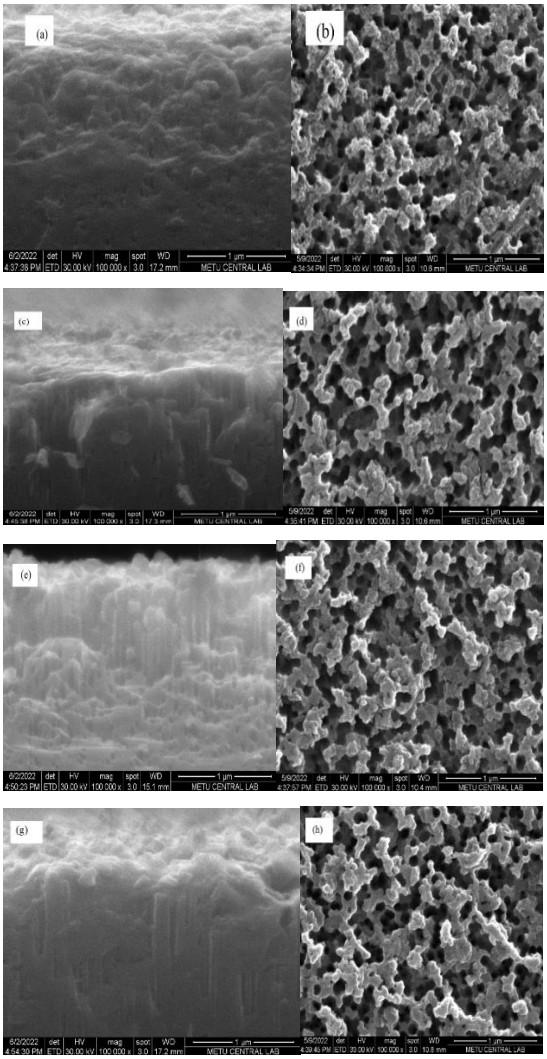


Figure 4. Cross sectional SEM images of SiNWs covered with Y_2O_3 thin films for (a) as deposited and annealead at (c) 200°C, (e) 400°C and (g) 600°C in N_2 for 40min while (b), (d), (f) and (h) are top views, respectively.

3.2. Annealing effects on Y_2O_3 thin films with SiNWs based on devices.

Figure 5, shows C-V curves measured at high frequency of 1MHz of MOS devices for as-deposited and annealed samples at 200°C, 400°C and 600°C. As may be noted from the C-V curves, the as-deposited possess highest capacitance value in the accumulation region compared to the annealed samples. However, as the annealing temperature increases, the capacitance value in the accumulation region found to decrease significantly. This could be due to the formation of interfacial layer between high-k material and silicon and dangling bonds during high annealing temperature [11]. Also, in the reduction of the surface morphologies of SiNWs as can be seen in Figure 2. Therefore, resulting in the reduction of the capacitance value and we have observed similar results in our earlier studies for Er_2O_3 thin films [9].

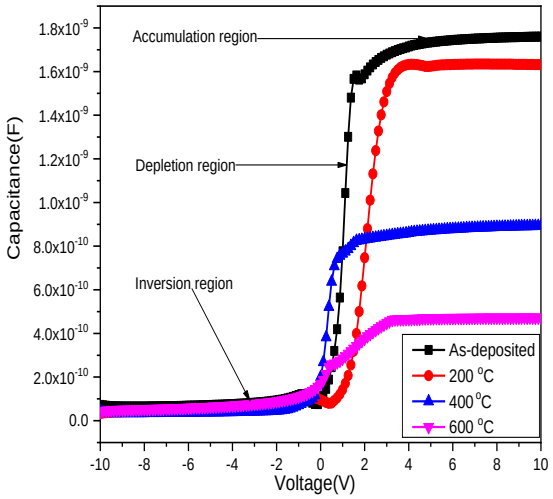


Figure 5. Measured capacitance-voltage(C-V) curves of $Al/Y_2O_3/SiNWs/n\text{-}Si/Al$ MOS capacitors as-deposited and annealed at 200°C, 400°C, and 600°C.

The dielectric constant(k) of as-deposited and annealed samples were extracted from the C-V curves and were calculated using the following equation [12]:

$$k = \left(\frac{C_{ox}t_{ox}}{\varepsilon_o A_{ox}}\right) \qquad (1)$$

where C_{ox}=C_{acc} is the value of oxide capacitance in the accumulation region, t_{ox} is the oxide thickness, $\varepsilon_\circ$ is the permittivity of free space and A_{ox} is gate electrode area of the MOS device.

The obtained k-values were found to be 16.8, 15.6, 8.5, and 4.5 for as deposited and annealed samples at 200°C, 400°C and 600°C. These values are also given Table 1. The reduction in the k-value with an increase of annealing temperature could be related to the existence of defects such as trap charges in the oxide layer [11], [12]. Also, the reduction in the accumulation capacitance value with an increase of annealing could lead to this behavior of dielectric constant. Moreover, the lowest (4.5) k value was obtained for the device annealed at 600°C and this value is comparable to the k (3.74) of CeO_2 [13]. However, the k(16.8) value of as-deposited can be also compared to the k(16.67) value found by earlier studies for Y_2O_3 thin films [14].

Table 1. Calculated electrical parameters of $Al/Y_2O_3/SiNWs/n\text{-}Si$ MOS capacitors for as-deposited and annealed samples at 200°C, 400°C and 600°C.

Temp (°C)	Q_{eff} (cm^{-2})	D_{it} (eV^{-1} cm^{-2})	ΔV_{fb} (V)	k
As-dep	-9.52×10^{11}	8.57×10^{10}	1.27	16.8
200	-1.72×10^{12}	2.29×10^{11}	2.71	15.6
400	-2.57×10^{11}	1.52×10^{10}	0.55	8.5
600	-4.88×10^{11}	3.98×10^{09}	2.66	4.5

From the C-V curves, the shift in the positive flat band voltage has been observed for as deposited and annealed samples. This kind of shift indicate that the negative effective oxide (Q_{eff}) charges are present in the oxide layer [11]. The Q_{eff} was obtained from the equation given below [12].

$$Q_{eff} = \frac{C_{ox}(W_{ms}-V_{fb})}{Aq} \qquad (2)$$

where W_{ms} is the work function difference between Al and Si, V_{fb} is the flatband voltage shift, q is the electronic charge, while other parameters have already been defined in Eq(1). The obtained Q_{eff} for as-deposited and annealed at 200°C, 400°C and 600°C are -9.52×10^{11} cm^{-2}, -1.72×10^{12} cm^{-2}, and $-2.57\times10^{11}cm^{-2}$. The value of Q_{eff} and ΔV_{fb} are also given in Table 1.

The value of density of states (D_{it}) was extracted from the C-V characteristics by using the conductance method. The value of D_{it} was determined by using the following below[9], [13].

$$D_{it} = \left(\frac{2}{qA}\right)\frac{G_{c,max/\omega}}{((G_c/\omega)/C_{ox})^2+(1-C_C/C_{ox})^2} \qquad (3)$$

where the G_c, max/ω is the corrected conductance corresponding to the maximum peak, C_c is the corrected capacitance, while other parameters have already been defined above.

The obtained value of D_{it} for as-deposited and devices annealed at 200°C, 400°C and 600°C are 8.57×10^{10} eV^{-1} cm^{-2}, 2.29×10^{11} eV^{-1} cm^{-2}, 1.52×10^{10} eV^{-1} cm^{-2}, 3.98×10^{09} eV^{-1} cm^{-2}. The values are also given in Table 1. As can be seen the value of D_{it} found to decrease with an increase in the annealing temperature. This may be charged to the formation of dangling bonds during high annealing temperature[9], [12], [13] Also, the reduction of D_{it} at for the device annealed at 600°C could be the formation of interfacial parasitic layer[4], [15].

4. Conclusion

In this study, we investigated the effect of annealing temperature on the structure, surface morphologies, and electrical properties of Y_2O_3 thin films with SiNWs. In the XRD spectra we observed that the sample annealed at 400°C was amorphous, in other words, no peak was present. On the other hand, we could not find any Ag peak in all XRD spectra. We also found that the surface morphologies of SiNWs with Y_2O_3 decreased significantly. The calculated electrical parameters such as the capacitance value in the accumulation, dielectric constant (k), density of states (D_{it}) decreased with an increase in the annealing temperature. Moreover, the positive shift in the V_{fb} voltage was observed and this could be related to the existence of negative effective charges in the oxide. The obtained Q_{eff} was in the range of $-2.57\times10^{11}cm^{-2}$ to $-1.72\times10^{12}cm^{-2}$.

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