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STRUCTURAL AND ELECTRICAL CHARACTERISTICS OF THE Al/Al_2O_3/SiO_2/n-SI METAL-OXIDE-SEMICONDUCTOR CAPACITOR

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Abstract. *In this study, the structural and electrical characteristics of the Al/Al_2O_3/SiO_2/n-Si Metal-Oxide-Semiconductor (MOS) structure were investigated. Al_2O_3 films were deposited on the n-type Si wafer by RF magnetron sputtering after the growth of SiO_2 by dry oxidation. The fabricated Al_2O_3/SiO_2/n-Si structures were annealed at 250°C, 450°C, and 750°C in a N_2 ambient. XRD and AFM measurements were conducted in order to examine the crystallinity and the surface topography of the Al_2O_3/SiO_2/n-Si structure. Aluminum (Al) front and back contacts were then deposited by RF magnetron sputtering. C-V and G/w-V measurements were performed at low and high frequencies with the aim of analyzing the electrical characteristics. The discrepancy in the C-V curves for different frequencies stemmed from the defects and dangling bonds at the interfaces and in the oxide layers.*

Keywords: *Trap charge density, thin films, defects, dangling bonds*

1. INTRODUCTION

Shrinking of microelectronics to nanoscale led to the research of alternatives for the conventional SiO_2 layer in the Metal-Oxide-Semiconductor (MOS) structure. This was mainly due to the increasing of the leakage currents associated with the SiO_2 layer as the entire structure shrank. The replacements had to possess a high dielectric constant in order to maintain a significant capacitance. Since then, high-k dielectrics have played an important role in MOS-based technology such as radiation sensors, and hence intensive research on these materials is ongoing [1]. The fabrication process of MOS capacitors involves unintentional and unavoidable establishment of crystal defects and impurities [2], which highly affect the entire device. They are usually described as dangling bonds, oxygen-vacancies, atom-like bonds, and anti-site defects and they are located at or very close to the oxide/semiconductor interface [3]. Therefore, reducing these defects and impurities is vital for the improvement of microelectronic devices.

In this study, Al_2O_3 was used as the gate oxide because it possesses a wide bandgap (8.6 eV), high dielectric constant (8.4), and suitable off-set values [4]. However, since SiO_2 still has an advantage of being electronically stable with Si, a thin layer of SiO_2 was deposited on Si before Al_2O_3 thin film deposition. Studies on the Al/Al_2O_3/Si capacitor and the Al/SiO_2/Si capacitor have been done [5]; it was found that the Al/Al_2O_3/Si capacitor was more sensitive to Co-Gamma radiation compared to the Al/SiO_2/Si. The reason was that the trapping in Al_2O_3 dielectric layer was more efficient [5]. In another study, annealing of the Al_2O_3/Si thin film led to the formation of the uncontrollable silicate layer [4] which can reduce the sensitivity of radiation sensors because of the signal fluctuations associated with it. Therefore, in order to reduce the formation of such layer, we introduced the SiO_2 layer before depositing Al_2O_3 on the Si wafer.

Radiation sensing highly depends on the material used. With this in mind, a structural analysis was done on the fabricated Al_2O_3/SiO_2/Si substrate with the aid of X-ray diffraction (XRD) and Atomic Force Microscopy (AFM). The electrical characteristics were also investigated by conducting C-V and G/w-V measurements. These measurements were performed for low and high frequencies in order to determine parameters such as barrier height (Φ_B) and dopant concentration (N_D).

2. EXPERIMENT

An n-type (100) Si wafer with the resistivity of 2-4 Ω-cm and the thickness of 500 μm underwent the standard RCA (Radio Corporation of America) cleaning process. A SiO_2 layer of approximately 15 nm was grown on the Si wafer by dry oxidation at 1000°C. Then, Al_2O_3 thin films of 90 nm thickness were deposited using the e-beam (electron beam) evaporator for 8 minutes at a base pressure of 4.8×10^{-4} Pa and the deposition temperature of 200°C. The wafer was divided into different parts and three of them were annealed at different temperatures, i.e. 250°C, 450°C and 750°C. Some parts were left as deposited (not annealed). X-ray diffraction (XRD) measurements were done for 4 samples, i.e. the as-deposited sample and those annealed at 250°C, 450°C, and 750°C. The measurements were done by an X-ray diffractometer (Miniflex, Rikagu, Japan) using Cu Kα radiation (λ = 1.5418 Å) at room temperature in the diffraction angle (2 θ) range of 20-80°. Aluminum circular front contacts of 1.5 mm in diameter were deposited on the Al_2O_3/SiO_2/Si structure. This deposition was done by

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placing a shadow mask on the samples before RF magnetron sputtering at 200W. The back contacts were deposited without the shadow mask. The whole fabrication process was done in the Class-100 clean room laboratories at the Nuclear Radiation Detectors Applications and Research Center, Bolu Abant Izzet Baysal University.

The *C-V* (capacitance-voltage) and *G/w-V* (conductance-voltage) characteristics were recorded by a computerized impedance analyzer (Keithley Semiconductor Characterization System 4200-SCS) in the voltage range of -10V to 10V for low and high frequencies.

3. Results and Discussion

XRD patterns of the $Al_2O_3/SiO_2/Si$ structure before and after annealing are shown in Fig. 1. Prior to annealing, the pattern consisted of only one Si peak. At low temperatures, a single peak is attributed to atoms not possessing sufficient mobility/energy to cause crystallization [6]. After annealing, another Si peak evolved and it became stronger as the annealing temperature increased. The absence of Al_2O_3 and SiO_2 peaks in all the patterns is consistent with the thin films being amorphous. It is reported that Al_2O_3 crystallizes at a high temperature (>900°C) [7].

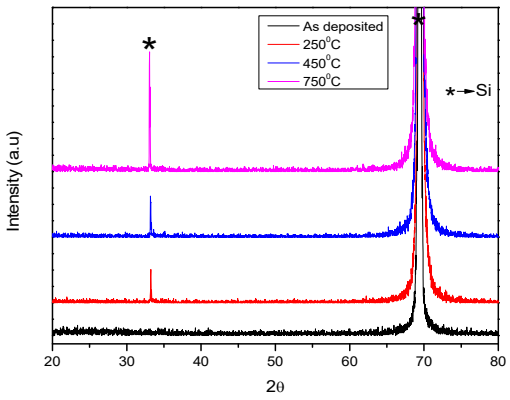

Figure 1. XRD patterns of the $Al_2O_3/SiO_2/Si$ structure as-deposited and annealed at 250°C, 450°C, and 750°C.

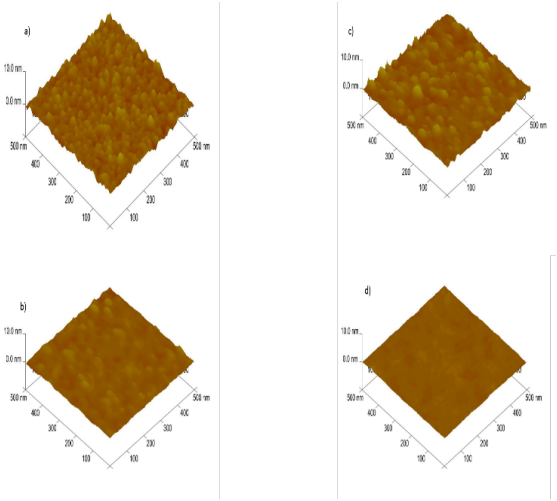

Figure 2. AFM images of a) as-deposited, b) 250 °C-annealed, c) 450 °C- annealed, and d) 750 °C-annealed Al_2O_3/SiO_2 films.

Topographic maps of the Al_2O_3/SiO_2 films were generated and analyzed using AFM (Atomic Force Microscopy). The size of the 3D AFM images is 500nm x 500nm, as shown in Fig. 2. Root-mean-square deviation (RMS) and Arithmetic-mean deviation (Ra) are ubiquitous parameters used in analyzing surface roughness. The RMS values for the Al_2O_3/SiO_2 films for as-deposited and those annealed at 250°C, 450°C and 750°C are 0.486, 0.298, 0.474, and 0.173, respectively. Furthermore, the Ra values are 0.380, 0.229, 0.361, and 0.138, respectively. The fact that the annealed films have the Ra and RMS values that are lower than those of the as-deposited film indicates that annealing helps to reduce surface roughness in the Al_2O_3/SiO_2 films.

C-V and G/w-V measurements are essential in analyzing the electrical characteristics of MOS capacitors. The deviations in the C-V and G/w-V curves stem mainly from series resistance and electrical charges trapped in the oxide and at the interface. Therefore, parameters that need to be determined include interfacial trap density (N_{it}), border trap density (N_{bt}), effective oxide trap density (N_{ox}), series resistance (R_s), etc. In order to analyze the electrical characteristics, we chose the sample annealed at 450°C since earlier on, Kimbugwe and Yilmaz [8] observed that its dielectric constant was the highest in comparison to the other samples and it had a flat-band voltage (-0.8V) that was the closest to the ideal one (~0.27 V) [8]. Here, we took these measurements for both low and high frequencies. Correction was done on the C-V and G/w-V measurements in order to eliminate the series resistance (R_S). The corrected measurements are shown in Fig. 3 and Fig. 4.

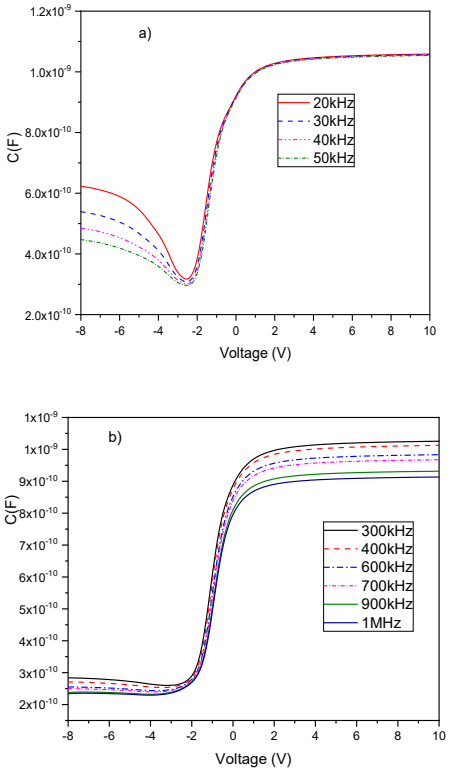

Figure 3. a) Low frequency and b) High frequency corrected C-V curves for the $Al_2O_3/SiO_2/Si$ MOS capacitor annealed at 450°C.

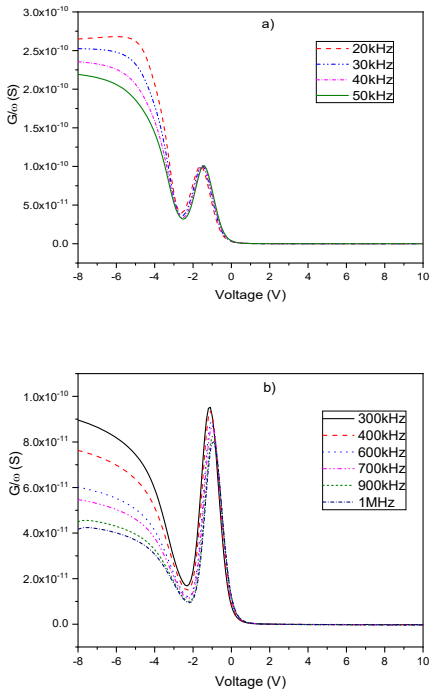

Figure 4.a) Low frequency and b) High frequency corrected G/w-V curves for the $Al_2O_3/SiO_2/Si$ MOS capacitor annealed at 450°C.

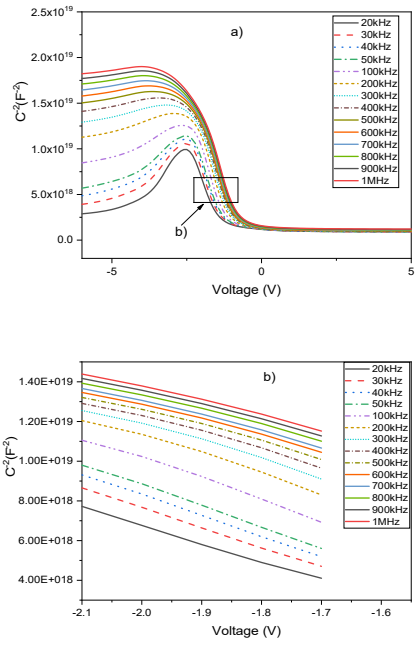

Figure 5. a) C^{-2}-V curves for the $Al_2O_3/SiO_2/Si$ MOS capacitor annealed at 450°C. b) Linear region of the C^{-2}-V curves for the $Al_2O_3/SiO_2/Si$ MOS capacitor annealed at 450°C.

In our previous study [8], N_{it}, N_{ox} and R_s dependence on frequency was analyzed. Here, we focused on analyzing the barrier height dependence on the frequency. Using the C^{-2}-V plots in Fig. 5, we obtained the barrier height (Φ_B) and dopant concentration (N_D).

In the depletion region, the capacitance of the MOS structure is given by [9][10]:

$$C_{dep} = \frac{\varepsilon_s A}{W_{dep}} \tag{1}$$

where $\varepsilon_s = k_s \varepsilon_o$ is the permittivity of the semiconductor (k_s = ~11.9 for Si), ε_o is the permittivity of the free space (8.854 x 10^{-12} F/m), and A is the area of the capacitor (1.77 x 10^{-2} cm²). The depletion layer width W_{dep} is given by [11]:

$$W_{dep} = \sqrt{\frac{2\varepsilon_s (V_O + V_g)}{qN_D}} \tag{2}$$

where V_O is the built-in potential, and N_D is the dopant concentration. Merging Eq. 1 and Eq. 2 results into [8][11]:

$$\frac{1}{C_{dep}^2} = \frac{2(V_o + V_g)}{qN_D \varepsilon_s A^2} \tag{3}$$

A linear variation in the C^{-2}-V curve appears in the depletion region, and the V_O value is obtained from where the line intersects with the voltage axis. Using the slope of the line, we can extract the dopant concentration N_D as shown in Eq. 4. [11]:

$$S = \frac{2}{qN_D \varepsilon_s S A^2} \tag{4}$$

The image force barrier lowering or barrier height reduction is the potential image charges induce in the metal contact after the voltage is applied at the gate. This potential has a tendency of reducing the effective barrier height; however, this reduction is lower than barrier height. The barrier height reduction can be obtained from Eq. 5. [12]

$$\Delta\Phi_B = \sqrt{\frac{qE_{\max}}{4\pi\varepsilon_s}} \tag{5}$$

where E_{max} is the maximum value of the electric field occurring as the result of the charge in the depletion region. It is assumed that this value is constant and it is given by:

$$E_{\max} = \sqrt{\frac{2qN_D(V_o - V_g)}{\varepsilon_s}} \tag{6}$$

For the n-type semiconductor-based MOS capacitor, the barrier height is expressed as [11]:

$$\Phi_B = V_o + \frac{k_g T}{q} + \frac{k_g T}{q}\ln\left(\frac{N_C}{N_D}\right) - \Delta\Phi_B \tag{7}$$

where N_C is the effective density of the states of conduction band (2.82 x 10^{19} cm^{-3}), and the diffusion potential, $V_D = V_o + k_B T/q$.

In ideal cases, the applied voltage does not affect the barrier height. But despite this, the barrier height is influenced by surface energy levels and interface traps that are present or evolve [11]. The Φ_B values shown in Table 1 are altered by these surface levels since they act like acceptors or ionized donors. In the n-type Si based MOS structure, as the negative interface trap charges (acceptor-like interface traps) lead to an increase in the Φ_B values because of the increasing positive space

charge density in the depletion region, the positive interface trap charges (donor-like interface traps) cause a decrease in the Φ_B values [11].

Table 1. Electrical parameters for the Al/Al2O3/SiO2/n-Si MOS capacitor annealed at 450°C

Frequency (kHz)	V_O (V)	V_D (V)	N_D (10^{15} cm^{-3})	E_F (eV)	$\Delta\phi_B$ (meV)	Φ_B (eV)
20	-1.26	-1.23	4.16	0.228	21.945	1.02
30	-1.23	-1.21	3.80	0.231	21.356	0.996
40	-1.20	-1.18	3.65	0.232	21.004	0.965
50	-1.17	-1.14	3.58	0.232	20.759	0.931
100	-1.02	-0.999	3.64	0.232	20.172	0.787
200	-0.80	-0.774	4.03	0.229	19.457	0.564
300	-0.63	-0.603	4.39	0.227	18.708	0.394
400	-0.50	-0.474	4.64	0.226	17.918	0.266
500	-0.33	-0.366	4.85	0.225	17.044	0.158
600	-0.37	-0.347	5.03	0.224	16.983	0.140
700	-0.26	-0.237	5.05	0.223	15.581	0.0288
800	-0.18	-0.150	5.19	0.223	14.201	0.0582
900	-0.13	-0.101	5.24	0.222	13.115	0.108
1000	-0.08	-0.0534	5.29	0.222	11.681	0.157

The Φ_B values obtained at high frequencies are low compared to those obtained at low frequencies. This indicates that at low frequencies more negative charges are trapped at the interface compared to positive charges. Furthermore, at high frequencies, more positive charges are trapped at the interface compared to negative charges. The high N_D values at high frequencies also support the fact that barrier height decreases since high donor charges associated with N_D attract many positive charges at the interface, hence reducing the barrier height.

4. Conclusion

Radiation interaction with a MOS structure results in the formation of charge trapping centers, hence some MOS structures can be used as foundations for radiation sensing devices. Heretofore, radiation sensing capabilities of the $Al/Al_2O_3/Si$ and $Al/SiO_2/Si$ were studied [5][13], and, after analyzing the structural and electrical characteristics of the $Al/Al_2O_3/SiO_2/Si$ capacitor, it can be regarded as a prospective radiation sensing capacitor. In this paper, the X-ray diffractometry results are consistent with the $Al_2O_3/SiO_2/Si$ layer being amorphous. Electrical parameters obtained include dopant concentration and barrier height. Carrier generation and recombination mechanisms at the interface traps on the oxide/semiconductor interface lead to a decline in the donor dopant concentration. At low frequencies, interface trapped charges can easily follow the AC signal; therefore, these mechanisms are enhanced. On the other hand, at high frequencies, interface trapped charges hardly follow the AC signal, meaning that such mechanisms are abated, causing an increase in the donor concentration (N_D). The high donor concentration at high frequencies also contributes to the reduction of the barrier height since high donor charges, associated with N_D, attract many positive charges to the interface.

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