FREQUENCY RESPONSE ON THE ELECTRICAL CHARACTERISTICS OF SiNWs BASED MOS CAPACITOR WITH HIGH-K MATERIAL

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Abstract. In this study we report the effect of different frequency on SiNWs based capacitor. The C-V and Gm/ω-V were carried at different frequency of 50 kHz to 1MHz. We found that the capacitance and conductance value decreased as the value of frequency increased and this was as a result of the distribution of interface trap charges in the dielectric layer. The effect of frequency on series resistance (Rsl) and interface states density (Dit) were investigated. It was found that the Rsl-V curves shifted toward the inversion region, while reducing in the accumulation region. The Dit value showed a decrease in the applied voltage frequency. After removing the effect of Rsl from C-V and Gm/ω-V curves, we found that the capacitance value increased significantly compared to uncorrected one, while the corrected conductance-voltage (Gc/ω-V) had peaks between 0.26V and 2.03V. Moreover, the obtained Dit value was on the order of 10¹⁰eV² cm⁻².

Keywords: MOS capacitor, SiNWs, interface state, capacitance-voltage

1. INTRODUCTION

Over the last decades, MOS capacitors have been investigated and applied in various fields. For instance, nanotechnology, radiation sensors and electronic devices [1]–[3]. However, it has been reported recently, device based on MOS capacitors possess low capacitance value in the accumulation region, this resulting in higher energy consumption and low speed for the devices based on MOS capacitors [4], [5]. Therefore, silicon nanowires (SiNWs) have received considerable attention from several research communities due to their electrical, optical and mechanical properties [6], [7].

Recently, different SiNWs fabrication procedures have been developed such as chemical vapor deposition (CVD), vapour liquid solid (VLS), laser ablation, metal assisted chemical etching (MACE) methods [7]. Among them, MACE is one of the easiest methods to fabricate SiNWs because one can be able to control surface morphology, orientation and length of nanowires and many more. In addition, this method can be performed at room temperature and it does not require dangerous gases and expensive equipment [6] [8].

Several authors have reported the fabrication of SiNWs based MOS capacitors. For instance, I. Leontis et al. obtained capacitance density of 2.6 μF/cm² with the length of SiNWs about 2.4 μm [1]. E. Hardakis et al. fabricated SiNWs based capacitor using SiO₂ as a dielectric layer. Their experimental results revealed that capacitor with SiNWs showed a higher capacitance density when compared to the one without SiNWs. This could be due to the etching process resulting in the increase in the capacitance density [9]. E. Nezasa et al. also reported the MOS capacitors with SiNWs using Al₂O₃ and TiO₂ as the high-k materials. The capacitance density of 5.9F/cm² was achieved at V = -4V and this was due to the combination of large surface of nanowires and high-k materials [5]. However, to the best of our knowledge there is no research that have been done so far on the frequency dependency of electrical characteristics of SiNWs based MOS capacitor with VOₓ as a oxide layer [10], [11]. Hence, in this research work, the effect of different frequency on MOS capacitors with SiNWs has been investigated intensively.

2. EXPERIMENTAL PROCEDURE

In this present work, we fabricated MOS capacitors with SiNWs by using n-type Si (100) wafers. The wafers had a resistivity in the range of 2-4 Ωcm and thickness 500μm. Firstly, the wafers were cleaned by using RCA cleaning processes. Secondly, the wafers were submerged in the mixed solution of AgNO₃/HF/H₂O (0.042g/9.6ml/50ml) for 2 minutes for the formation of silver nanoparticles (AgNPs). Thirdly, the Si wafers that had AgNPs were immersed in a solution consisting with HF/H₂O₂/H₂O (8ml/2ml/80ml) for 15 minutes in order to etch the samples. Fourthly, the etched samples were drenched in a mixture of HNO₃/H₂O for the removal of AgNPs. Prior to the deposition of Vanadium oxide (VO₂) thin films. The oxide layer that might be grown during the fabrication of SiNWs was removed from the samples by using HF/H₂O (50ml/100ml) for 60 seconds. Finally, the silicon wafers with SiNWs were transferred into a magnetron sputtering system for the deposition

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of VO₂ thin films. The substrate temperature was set at 100°C, the deposition pressure was ~5.9×10⁻⁴ Pascal (Pa), pres-spatter was 20 min, sputtering time was 30 min and sputtering power was 250 Watts. The thickness of VO₂ was determined by measuring using the sun spectrometer reflectometer and the thickness was found to be 145 nm. The samples with VO₂ thin films were again transferred to the RF sputtering system for the purpose of forming both gate electrodes and back contact using Aluminium as a sputtering target and for more information readers are referred to [2]. After all the fabrication processes were completed the C-V measurements were carried out in the frequency ranging from 50 kHz to 1 MHz and the voltage was set between -10 V and +10 V. The fabricated MOS capacitors based on SiNWs is given in Figure 1.

![Figure 1. Schematic structure of the fabricated Al/VO₂/SiNWs/MOS capacitors](image)

3. RESULTS AND DISCUSSION

3.1. Elemental composition and surface morphologies analysis

Energy dispersive spectroscopy (EDS) system was used to study the elemental compositions of SiNWs etched for 12 min (a) and (b) after deposition of VO₂ thin films onto SiNWs/n-Si (100) and the sample was annealed at 400°C in N₂ for 40 min. It can be seen that only three elements are present namely; oxygen, silicon and vanadium. As shown in Fig. 2 (a) and (b), oxygen and silicon possess emission x-ray signals Kα at 0.96 eV and 1.97 eV while vanadium has Kα at 4.5 eV and Kβ at 5.3 eV.

Figure 3 shows cross sectional (a) and (b) top view of SiNWs. The SEM image well aligned SiNWs in the vertical direction and distributed almost uniformly over the surface of a silicon substrate. On the other hand, top view forms some bundles. The reason behind this is due to mutual interaction of SiNWs and dangling bonds [8], [12], [13]. However, after deposition of VO₂ thin films onto SiNWs, we found that surface morphologies of SiNWs reduced significantly Figure 3 (c) and (d). The main reason behind this may be due to the penetration of VO₂ thin films into SiNWs pillars.

![Figure 2. EDS spectra of (a) SiNWs etched for 12 min and (b) after deposition of VO₂ thin films onto SiNWs/n-Si (100) for annealed sample at 400°C in N₂ for 40 min.](image)

![Figure 3 (a). Cross sectional view SEM image of SiNWs.](image)
3.2. Electrical characteristics

Figure 4 (a), explains the C-V curves of Al/VO$_2$/SiNWs MOS device at different frequency of range 50 kHz to 1MHz. As may be illustrated from the C-V curves, there are three types of regions, namely: accumulation, inversion, depletion region. The value of capacitance in the accumulation region decreased when there is an increase in the applied voltage frequency. It is a known fact that interface trap charges can much more easily follow the ac signal at low frequency and contribute to the capacitance in the accumulation region [12], [13]. However, at high frequency these charges do not have sufficient time to respond effectively to the voltage being applied due to their larger life time. In other words, the contribution of the capacitance in the accumulation region is negligible [2], [9], [14].

\[
R_s = \frac{G_m}{\omega (\omega C_m)^2}
\]
where $C_m$ is the value of capacitance and $G_m$ is the value of conductance in the accumulation region and $\omega = 2\pi f$ corresponds to the angle or frequency.

Figure 5 (a), illustrates the series resistance voltage ($R_s$-$V$) of Al/VO$_2$/SiNWs/n-Si MOS capacitor at different frequency of 50 kHz to 1MHz. As it can be seen, the value of $R_s$ decreased in the accumulation. On the other hand, these values shifted towards the inversion region this could be related to the various charges such as interface trap charge and oxide charge [15], [18].

![Series Resistance ($) vs Voltage ($V$) for Al/VO$_2$/SiNWs/n-Si MOS Cap]  

The values of interface states density ($D_{it}$) were calculated from the following equations[2], [17].

$$D_{it} = \frac{2}{qA} \left( \frac{G_{m, max/\omega}}{(G_{C}/\omega)/C_{ox}} \right) + (1 - C_{L}/C_{ox})^{2}$$

(2)

In the equation, $q$ is the electron charge, $A$ represents area of gate electrode device $G_m/\omega$-$V$ corrected conductance which corresponds to the maximum peak. $C$ represents the corrected capacitance and $C_{ox} = C_{max}$ is the capacitance value in the accumulation region in other words, is an oxide capacitance value in the strong accumulation region.

The interface states density as function of frequency has been plotted in Fig. 5 (b), it has been observed that interface states decreased with an increase in the applied voltage frequency. As stated before in Fig. (3a) the interface states can easily follow the ac signal at low frequency while at high frequency these charges cannot follow the ac signal due to their large time life[1], [2], [16].

![Interface States Density ($) vs Voltage ($V$) for Al/VO$_2$/SiNWs/n-Si MOS Cap]  

The C-V and $G_m/\omega$-$V$ measurements were corrected by using the $R_s$ values from the strong accumulation. The values of $C_c$ and $G_m/\omega$-$V$ were calculated using the following expression [2], [14].

$$C_c = \frac{(G_m)^2(\omega C_m)^2}{\alpha^2 + (\omega C_m)^2}$$

(3)

$$G_c = \frac{(G_m)^2 + (\omega C_m)^2}{\alpha^2 + (\omega C_m)^2}$$

(4)

$$a = G_m - \left[ G_m^2 + (\omega G_m)^2 \right] R_s$$

(5)

The C-V and $G_m/\omega$-$V$ curves were corrected for the effect of $R_s$ as shown Fig. 6 (a) and (b). After removing the effect of $R_s$ in Fig. 5 (a), we found that the corrected capacitance-voltage curves increased significantly compared to uncorrected ones in Fig. 4 (a). On the other hand, corrected conductance voltage ($G_m/\omega$-$V$) curves had peaks and these peaks were between 0.26V and 2.03 V as compared to Figure 4 (b). Moreover, in Figure 6 (b), the peaks decreased with increasing applied voltage frequency and this could be related of interface trap charges as stated before. Therefore, we observed that $R_s$ had a huge influence on the C-V and $G_m/\omega$-$V$ curves.

![Corrected Capacitance ($) vs Voltage ($V$) for Al/VO$_2$/SiNWs/n-Si MOS Cap]  

Conclusion

In the investigative study, we comprehensively analysed the effect of frequency on the C-V and $G_m/\omega$-$V$ curves. We found that the C-V value in the accumulation was inversely related to the applied voltage frequency, it decreased while voltage increased.
This was attributed to the distribution of interface trap charges inside the dielectric material. These R-V value decreased in the accumulation and then shifted towards the inversion region, while the Dn decreased with an increase in the frequency. Moreover, after removing the effect of Rf from C-V and Gm/o-V curves, we observed that the C-V curves increased significantly compared to uncorrected ones, while the Gm/o-V had peaks between 0.23 V and 2.6 V.

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